Appln. No.: 10/810,607

Amendment dated August 30, 2004

Reply to Office Action of June 3, 2004

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-2 (canceled)

Claim 3 (currently amended): A method of replacing a defective memory cell comprising:

comparing an input address with a defective address stored in a plurality of storage circuits, the defective address assigned to a defective memory cell in a plurality of memory blocks; and

replacing defective memory cells in the plurality of memory blocks with one of a plurality of redundancy units, based on mapping information indicative of a relationship with the redundancy units stored in the storage circuits when the input address matches the defective address,

The method according to claim 2, wherein the number of storage circuits is smaller than the number of redundancy units.

Claim 4 (currently amended): A method of replacing a defective memory cell comprising:

comparing an input address with a defective address stored in a plurality of storage circuits, the defective address assigned to a defective memory cell in a plurality of memory blocks; and

replacing defective memory cells in the plurality of memory blocks with one of a plurality of redundancy units, based on mapping information indicative of a relationship with the redundancy units stored in the storage circuits when the input address matches the defective address,

The method according to claim 2, wherein each of the redundancy units is located adjacent to a corresponding one of the plurality of memory blocks.

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Claim 5 (currently amended): A method of replacing a defective memory cell comprising:

comparing an input address with a defective address stored in a plurality of storage circuits, the defective address assigned to a defective memory cell in first memory blocks,

second memory blocks being activated independently of the first memory blocks; and

replacing defective memory cells in the first memory blocks with one of a plurality of

first redundancy units, and defective memory cells in the second memory blocks with one of a

plurality of second redundancy units, based on mapping information indicative of a relationship

with the first and second redundancy units stored in the storage circuits when the input address

matches the defective address.

Claim 6 (previously presented): The method according to claim 5, wherein the number of

storage circuits is smaller than the number of first and second redundancy units.

Claim 7 (previously presented): The method according to claim 5, wherein each of the first

redundancy units is located adjacent to a corresponding one of the first memory blocks and each

of the second redundancy units is located adjacent to a corresponding one of the second memory

blocks.

Claim 8 (currently amended): A method of replacing a defective memory cell comprising:

comparing an input address with a defective address stored in a plurality of storage

circuits, the defective address assigned to a defective memory cell in a plurality of memory

blocks each to be activated independently; and

replacing defective memory cells in the plurality of memory blocks with one of a

plurality of redundancy units, based on mapping information indicative of a relationship with the

redundancy units stored in the storage circuits when the input address matches the defective

address.

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Claim 9 (previously presented): The method according to claim 8, wherein the number of storage circuits is smaller than the number of redundancy units.

Claim 10 (previously presented): The method according to claim 8, wherein each of the redundancy units is located adjacent to a corresponding one of the plurality of memory blocks.